UNITED STATES PATENT APPLICATION

FOR

PRECISE PATTERNING OF HIGH-K FILMS

Inventors: Justin K. Brask
Mark L. Doczy
Matthew V. Metz
John Barnak
Paul R. Markworth

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

Attorney Docket No.: 42P15696

"Express Mail" mailing label number: EV 336 583 947 US
Date of Deposit: August 1, 2003
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
Teresa Edwards
(Typed or printed name of person mailing paper or fee)
Teresa Edwards
(Signature of person mailing paper or fee)
August 1, 2003
(Date signed)

PRECISE PATTERNING OF HIGH-K FILMS

FIELD OF THE INVENTION

[0001] This invention relates to fabricating microelectronic devices, and more particularly to precision formation of a trench in a dielectric layer.

BACKGROUND OF THE INVENTION

[0002] Microelectronic structures, such as semiconductor structures, may be created by forming layers and trenches in various structural configurations from various materials. One of the challenges associated with conventional techniques utilized for patterning dielectric films, such as high dielectric constant, or "high-K", films is trenching with accuracy to avoid damage to the integrity of adjacent structures. Referring to Figure 1A, a cross-sectional view of a typical gate structure is depicted wherein two gates (104, 106) with spacers (108, 110, 112, 114) are formed adjacent a high-K gate oxide layer (102), which is formed adjacent a substrate layer (100). Figure 1B depicts an undesirable patterning scenario wherein dry etching techniques have been utilized, resulting in a trench (116) that is overdeep. While the relatively anisotropic properties of dry etching techniques are favored for minimizing negative etch bias, they may be associated with difficulty in controlling trenching depth, as depicted, for example, in Figure 1B, where the trench (116) extends undesirably into the substrate layer (100). Figure 1C depicts another undesirable patterning scenario wherein wet etching has been utilized, resulting in a trench (118) that undesirably undercuts neighboring structures such as gates (104, 106) and spacers (110, 112). Many wet etching treatments are associated with substantially isotropic etch rate characteristics, resulting in negative etch bias and undercutting, as depicted, for example, in Figure 1C.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The present invention is illustrated by way of example and is not limited in the figures of the accompanying drawings, in which like references indicate similar elements. Features shown in the drawings are not intended to be drawn to scale, nor are they intended to be shown in precise positional relationship.

[0004] Figures 1A-1C are cross-sectional depictions of conventional substrate patterning treatment.

[0005] Figures 2A-2C are cross sectional views of various aspects of a patterning treatment of an embodiment of the present invention.

[0006] Figure 3 is a flowchart depicting various stages of a patterning treatment of an embodiment of the present invention.

[0007] Figures 4A-4D are cross sectional views of various aspects of a patterning treatment of a second embodiment of the present invention.

[0008] Figure 5 is a flowchart depicting various stages of a patterning treatment of the second embodiment of the present invention.

DETAILED DESCRIPTION

[0009] In the following detailed description of embodiments of the invention, reference is made to the accompanying drawings in which like references indicate similar elements. The illustrative embodiments described herein are disclosed in sufficient detail to enable those skilled in the art to practice the invention. The following detailed description is therefore not to be taken in a limiting sense, and the scope of the invention is defined only by the appended claims.

[0010] Figures 2A-2C are cross sectional views of various aspects of a patterning treatment of one embodiment of the present invention. Referring to Figure 2A, a microelectronic structure similar to that depicted in Figure 1A is shown. Such a structure may be formed utilizing various techniques and materials. For example, a high-K dielectric layer (102) may be formed upon a substrate layer (100) using techniques such as chemical or physical vapor deposition or other techniques. In various embodiments, the high-K dielectric layer (102) may comprise a high-K material such as hafnium dioxide, zirconium dioxide, or silicate derivatives thereof, and the substrate layer (100) may comprise a semiconducting material such as silicon, or another material. Subsequently, gates (104, 106) may be formed between spacers (108, 110, 112, 114). In an embodiment, the gates (104, 106) comprise a gate material such as polysilicon and the spacers (108, 110, 112, 114) comprise a spacer material such as silicon nitride, although other materials may be used in other embodiments. Subsequent to formation of the gates (104, 106) and spacers (108, 110, 112, 114), a portion (132) of the high-K dielectric layer (102) surface remains exposed.

[0011] Referring to Figure 2B, the exposed high-K dielectric layer surface (132) is exposed to hydrogen (120), resulting in a hydrogen reduction reaction. Reduction of d-block (between groups II and III on the Periodic Table) transition metal complexes/films with molecular hydrogen to the corresponding metallic species is a well-known phenomenon, described, for example, in publications such as "Chemistry of the Elements", 2nd Edition, by N. N. Greenwood and A. Earnshaw, 1997.

Hydrogen tunnels in the direction in which it is applied easily into such films to depths commonly encountered in high-K microelectronic device structures, such as between about 5 and about 100 angstroms, in a substantially anisotropic manner.

[0012] In an embodiment, the exposed surface (132) is exposed to hydrogen (120) in a parallel plate plasma chamber, where a device wafer that includes the gates (104, 106), high-K dielectric layer (102), and substrate layer (100) acts as one plate, and is spaced in a range of about 5 mm to about 10 mm from a second plate. There is a radio frequency ("RF") power source with a power density in a range of about 2 W/cm^2 to about 4 W/cm^2, and a frequency in a range of about 200 kHz to about 13.5 MHz. The temperature of the wafer is in a range from about 20° C to about 450° C. There is a hydrogen flow rate in a range of about 1000 SCCM to about 2000 SCCM and a flow rate of an inert gas such as argon or helium in a range of about zero SCCM to about 2000 SCCM. The chamber has a pressure in a range of about 1 Torr to about 2 Torr. Other embodiments may use different conditions to perform the hydrogen reduction reaction.

[0013] In an embodiment wherein the high-K gate dielectric (102) comprises hafnium dioxide, the hydrogen reduction reaction may be notated as follows:

$$HfO_2 + 2H_2 \rightarrow Hf + 2H_2O$$

[0014] The result of the reduction reaction is a reduced portion (122) of the high-K gate dielectric layer (102). The reduced, or "converted" portion (122), now a metallic substance, may be selectively removed, as depicted in Figure 2C, via exposure to a wet etch chemistry (124) selective to the converted metallic, such as the sulfuric acid and hydrogen peroxide based etch chemistry known as a "piranha" etch chemistry, or a hydrochloric acid and hydrogen peroxide based wet etch chemistry known as an "SC2" or "RCA standard clean 2" wet etch chemistry, to leave behind a trench (126). Removal of the reduced portion (122) also results in remaining discrete portions (128, 130) of the high-K dielectric layer (102). The trench (126) is without substantial negative etch bias or damage to the underlying substrate layer (100) due to the relatively high selectivity of such wet

etch chemistry (124) to metallics as opposed to other adjacent nonmetallic materials, including adjacent portions of the high-K gate dielectric (102) which have not been reduced or converted. Indeed, the trench (126) resulting from the removal of reduced material (122) is substantially straight with substantially parallel walls - also known in the art as a trench having substantially zero positive or negative "etch bias." Wet etch chemistries (124) such as piranha and SC2 are well known in the art as systems for selectively removing organics and metallics to reach underlying metallic or substrate materials. For example, a low pH system with an oxidant, such as hydrochloric acid with peroxide as in the SC2 etch chemistry, is a known effective way to dissolve metallics. In other embodiments, other methods such as an aqueous solution of a common chelating agent, derivatives of phosphonates or ethylenediaminetetraacetic acid for example, may be used to selectively remove the reduced portion (122). Thus, the dielectric layer (102) is patterned with precision to avoid problems with eroding an underlying substrate layer (100) and undercutting adjacent structures, such as gates (104, 106) or spacers (108, 110, 112, 114).

[0015] Referring to Figure 3, a flowchart summarizing a patterning treatment of one embodiment of the present invention is depicted, wherein a high-K gate dielectric layer is formed (300) adjacent a substrate layer, subsequent to which gates and spacers are formed (302) adjacent the high-K gate dielectric layer, leaving an exposed surface of the high-K gate dielectric layer. The exposed high-K gate dielectric layer surface is exposed (304) to hydrogen gas, which leads to a reduction reaction. The reduced high-K gate dielectric material is etched (306) to form a trench by a wet etch chemistry that is selective to the reduced high-K gate dielectric material so that the reduced gate dielectric material is selectively removed without substantially undercutting adjacent gate structures or substantially eroding underlying substrate layer materials.

[0016] Figures 4A-4D are cross sectional views of various aspects of a patterning treatment of a second embodiment of the present invention. Referring to Figure 4A, a microelectronic structure similar to that depicted in Figure 2A is shown. However, the structure in Figure 4A does not include

spacers (108, 110, 112, 114) adjacent the gates (104, 106). Such a structure may be formed utilizing various techniques and materials. For example, a high-K dielectric layer (102) may be formed upon a substrate layer (100) using techniques such as chemical or physical vapor deposition or other techniques. In various embodiments, the high-K dielectric layer (102) may comprise a high-K material such as hafnium dioxide, zirconium dioxide, or silicate derivatives thereof, and the substrate layer (100) may comprise a semiconducting material such as silicon, or another material. Subsequently, gates (104, 106) may be formed on the high-K dielectric layer (102). In an embodiment, the gates (104, 106) comprise a gate material such as polysilicon, although other materials may be used in other embodiments. Subsequent to formation of the gates (104, 106), a portion (132) of the high-K dielectric layer (102) between the gates (104, 106) remains exposed.

[0017] Referring to Figure 4B, the exposed high-K dielectric layer surface (132) is exposed to hydrogen (120), resulting in a hydrogen reduction reaction. In an embodiment, this exposure is performed similarly to the exposure described above with respect to Figure 2B, with the same result of a reduced portion (122) of the high-K gate dielectric layer (102). The reduced, or "converted" portion (122), now a metallic substance, may be selectively removed, as depicted in Figure 4C, via exposure to a wet etch chemistry (124) selective to the converted metallic to leave behind a trench (126). This wet etch chemistry (124) is typically performed in the same manner as described above with respect to Figure 2C. Removal of the reduced portion (122) also results in remaining discrete portions (128, 130) of the high-K dielectric layer (102). The trench (126) is without substantial negative etch bias or damage to the underlying substrate layer (100) due to the relatively high selectivity of such wet etch chemistry (124) to metallics as opposed to other adjacent nonmetallic materials, including adjacent portions of the high-K gate dielectric (102) which have not been reduced or converted. Indeed, the trench (126) resulting from the removal of reduced material (122) is substantially straight with substantially parallel walls - also known in the art as a trench having substantially zero positive or negative "etch bias." Thus, the dielectric layer (102) is patterned with

precision to avoid problems with eroding an underlying substrate layer (100) and undercutting adjacent structures, such as gates (104, 106).

[0018] Referring to Figure 4D, spacers (108, 110, 112, 114) are then formed adjacent to the gates (104, 106) and the discrete portions (128, 130) of the high-K dielectric layer (102). As shown in Figure 4D, spacers (110, 112) are formed adjacent to both gates (104, 106) and discrete portions (128, 130) of the high-K dielectric layer (102), and extend from substantially a top surface of the gates (104, 106) into the trench (126) and to a top surface of material exposed by removal of the reduced portion (122) of the high-K dielectric layer (102). The top surface of material exposed by removal of the reduced portion (122) of the high-K dielectric layer is the bottom surface of the trench, which is the top surface of the substrate layer (100) in the illustrated embodiment. In an illustrated embodiment, a trench (126) is formed on one side of each of the gates (104, 106). The high-K dielectric layer (102) remains on a non-trench side of the gates (104, 106). In such an embodiment, spacers (108, 114) on the non-trench side of the gates (104, 106) are formed adjacent to the gates (104, 106) and extend from substantially the top surface of the gates (104, 106) to top surfaces of the discrete portions (128, 130) of the high-K dielectric layer (102). In other embodiments (not illustrated) however, trenches (126) may be formed on both sides of one or both of the gates (104, 106). In these other embodiments, one or both of spacers (108, 114) on the non-trench side of the gates (104, 106) may also be formed adjacent to both gates (104, 106) and discrete portions (128, 130) of the high-K dielectric layer (102), and extend from substantially a top surface of the gates (104, 106) into the trench (126) and to a top surface of the substrate layer (100) exposed by removal of the reduced portion (122) of the high-K dielectric layer (102). Thus, the dielectric layer (102) is patterned with precision to avoid problems with eroding an underlying substrate layer (100) and undercutting adjacent structures, such as gates (104, 106) or spacers (108, 110, 112, 114).

[0019] Referring to Figure 5, a flowchart summarizing a patterning treatment of one embodiment of the present invention is depicted, wherein a high-K gate dielectric layer is formed

(500) adjacent a substrate layer, subsequent to which gates are formed (502) adjacent the high-K gate dielectric layer, leaving an exposed surface of the high-K gate dielectric layer. The exposed high-K gate dielectric layer surface is exposed (504) to hydrogen gas, which leads to a reduction reaction. The reduced high-K gate dielectric material is etched (506) to form a trench by a wet etch chemistry that is selective to the reduced high-K gate dielectric material so that the reduced gate dielectric material is selectively removed without substantially undercutting adjacent gate structures or substantially eroding underlying substrate layer materials. Then, spacers are formed (508) adjacent the gates and a portion of the remaining high-K gate dielectric layer. On sides of the gates adjacent the trench, these spacers extend substantially from the top surface of the gates to the top surface of the substrate layer.

[0020] Thus, a novel substrate patterning solution is disclosed. Although the invention is described herein with reference to specific embodiments, many modifications therein will readily occur to those of ordinary skill in the art. Accordingly, all such variations and modifications are included within the intended scope of the invention as defined by the following claims.